Confirmation No. 8030 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	VAN SCHAIJK *et al.*	Examiner:	Hsieh, H.
Serial No.:	10/574,030	Group Art Unit:	2811
Filed:	March 27, 2006	Docket No.:	NL031167US1 (NXPS.442PA)

Title: TWO-TRANSISTOR MEMORY CELL AND METHOD FOR MANUFACTURING

APPEAL BRIEF

Mail Stop Appeal Brief-Patents
Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Customer No.
65913

Dear Sir:

This Appeal Brief is submitted pursuant to 37 C.F.R. §41.37, in support of the Notice of Appeal filed October 25, 2010 and in response to the rejections of claims 1, 3-7, 14 and 17-19 as set forth in the Final Office Action dated July 26, 2010.

Please charge Deposit Account number 50-4019 (NL031167US1) $540.00 for filing this brief in support of an appeal as set forth in 37 C.F.R. §1.17(c). If necessary, authority is given to charge/credit Deposit Account 50-4019 additional fees/overages in support of this filing.

I. Real Party In Interest

The real party in interest is NXP Semiconductors. The application is presently assigned of record, at reel/frame nos. 019719/0843 to NXP, B.V., headquartered in Eindhoven, the Netherlands.

II. Related Appeals and Interferences

While Appellant is aware of other pending applications owned by the above-identified Assignee, Appellant is unaware of any related appeals, interferences or judicial proceedings that would have a bearing on the Board's decision in the instant appeal.

III. Status of Claims

Claims 1, 3-7, 14 and 17-19 stand rejected and are presented for appeal. Claims 2, 9 and 12 are cancelled and claims 8, 10-11, 13 and 15-16 are withdrawn. A complete listing of the claims under appeal is provided in an Appendix to this Brief.

IV. Status of Amendments

An Amendment and Response to Office Action was filed on September 27, 2010, in response to the Office Action dated July 26, 2010. The Advisory Action dated October 15, 2010 notes that the amendment was entered. No further amendments have been filed.

V. Summary of Claimed Subject Matter

As required by 37 C.F.R. § 41.37(c)(1)(v), a concise explanation of the subject matter defined in the independent claims involved in the appeal is provided herein. Appellant notes that representative subject matter is identified for these claims; however, the abundance of supporting subject matter in the application prohibits identifying all textual and diagrammatic references to each claimed recitation. Appellant thus submits that other application subject matter, which supports the claims but is not specifically identified above, may be found elsewhere in the application. Appellant further notes that this summary does not provide an exhaustive or exclusive view of the present subject matter, and Appellant refers to the appended claims and their legal equivalents for a complete statement of the invention.

Commensurate with independent claim 1, a method of manufacturing, on a substrate (*see, e.g.*, Figs. 5, 6, 8, 9 and 10, reference 50), a two-transistor memory cell including a storage transistor (*see, e.g.*, Fig. 10, reference 1 and 2, and page 3:8) having a memory gate stack (*see, e.g.*, Fig. 10, reference 1) and a selecting transistor (*see, e.g.*, Fig.10, reference 2), there being a tunnel dielectric layer between the substrate and the memory gate stack(*see, e.g.*, Fig. 10, reference 51, and page 3:8-10), is disclosed. The method includes forming the memory gate stack by, providing a first conductive layer on the tunnel dielectric layer (*see, e.g.*, Fig. 10 reference 52) and a second conductive layer (*see, e.g.*, Fig. 10, reference 54) with a deposited interlayer dielectric layer between the first and second conductive layers (*see, e.g.*, Fig. 10, reference 53), the deposited interlayer dielectric layer including oxide and being susceptible to undesirable growth upon exposure to oxygen during subsequent oxidation steps (*see, e.g.*, page 7:20-29 and page 8:28-32). The method further includes etching the second conductive layer thus forming a control gate (*see, e.g.*, page 8:3 and 7-17). Next, spacers (*see, e.g.*, Fig. 10, reference 81) are formed against the control gate in the direction of a channel to be formed under the tunnel dielectric layer (*see, e.g.*, page 8:17-19). The spacers are formed from a dielectric material having an oxygen diffusion through the dielectric material that is, relative to oxide spacers, an order of magnitude smaller than oxygen diffusion through the oxide spacers (*see, e.g.*, page 9:5-10). Thereafter, the spacers are used as a hard mask to etch the first conductive layer thus forming the floating gate, the etching of the first conductive layer being an anisotropic dry etch that is selective to the tunnel dielectric (*see, e.g.*, page 9:14-19), thereby using the tunnel dielectric to protect portions of the substrate laterally adjacent to the floating gate (*Id.*). The method includes removing a portion of the tunnel dielectric laterally adjacent to the floating gate and exposing a portion of the substrate where the tunnel dielectric has been removed (*see, e.g.*, page 9:20-22). The method also includes forming an access gate dielectric oxide on the exposed portion of the substrate (*see, e.g.*, Fig. 10, reference 101), using the spacers to mitigate the diffusion of oxygen to the deposited interlayer dielectric layer (*see, e.g.*, Fig. 9).

Commensurate with independent claim 17, a method of manufacturing a two-transistor memory cell comprising a storage transistor having a memory gate stack and a selecting transistor (*see, e.g.*, Fig. 10, references 1 and 2). The method includes forming a

tunnel dielectric on a substrate (*see, e.g.*, Fig. 10, reference 51), forming a first conductive layer on the tunnel dielectric (*see, e.g.*, Fig. 10, reference 52), and depositing an interlayer dielectric layer on the first conductive layer (*see, e.g.*, Fig. 10, reference 53). The deposited interlayer dielectric layer including oxide and being susceptible to undesirable growth upon exposure to oxygen during subsequent oxidation steps (*see, e.g.*, page 7:20-29 and page 8:28-32). The method further includes forming a second conductive layer on the interlayer dielectric layer (*see, e.g.*, Fig. 10, reference 54) and etching the second conductive layer to form a control gate (*see, e.g.*, page 8:3 and7-17). The method includes forming a selecting transistor on the substrate laterally adjacent to the first conductive layer and having an access gate on an access gate dielectric (*see, e.g.*, Fig. 10, references 101 and 103). The method includes forming spacers against sides of the control gate (*see, e.g.*, Fig. 10, reference 81), the spacers being formed from a dielectric material having an oxygen diffusion through the dielectric material that is, relative to oxide spacers, an order of magnitude smaller than oxygen diffusion through the oxide spacers (*see, e.g.*, page 9:5-10), one of the spacers being formed between the control gate and the access gate (*see, e.g.*, Fig. 10). The spacers are used to mask underlying portions of the interlayer dielectric layer and the first conductive layer (*see, e.g.*, *Id.)*, etching the first conductive layer to form a floating gate using an anisotropic dry etch that is selective to the tunnel dielectric, using the tunnel dielectric to mask portions of the substrate laterally adjacent to the floating gate (*see, e.g.*, page 9:14-19). The method includes forming a floating gate sidewall dielectric that is contiguous with the access gate dielectric and present between the floating gate and the access gate, wherein the one of the spacers being formed between the control gate and the access gate is thicker than the floating gate sidewall dielectric (*see, e.g.*, Fig. 10 and page 9:22-29). The method includes removing a portion of the tunnel dielectric laterally adjacent to the floating gate and exposing a portion of the substrate where the tunnel dielectric has been removed (*see, e.g* Fig. 9). The method includes forming an access gate dielectric oxide on the exposed portion of the substrate and using the spacers to mitigate the diffusion of oxygen to the deposited interlayer dielectric layer (*see, e.g.*, page 9:20-22).

VI. Grounds Of Rejection To Be Reviewed Upon Appeal

The grounds of rejection to be reviewed on appeal are as follows:

A. Claims 1, 3, 5, 7 and 17-19 stand rejected under 35 U.S.C. § 103(a) over Chang (U.S. Patent No. 5,991,204) in view of Sharma (U.S. Patent 5,488,579) and further in view of a Quirk reference ("Semiconductor Manufacturing Technology").

B. Claims 4 and 14 stand rejected under 35 U.S.C. § 103(a) over the '204, '579 and Quirk references and further in view of Hong (U.S. Patent No. 5,614,746).

C. Claim 6 stands rejected under 35 U.S.C. § 103(a) over the '204, '579 and Quirk references and further in view of Chen (U.S. Patent No. 6,091,104).

VII. Argument

A. The Rejection Of Claims 1, 3-7, 14 and 17-19 Is Improper

1. The Rejection Is Improper For Lack of Correspondence

The § 103(a) rejections are improper because the cited combination of references lacks correspondence. For example, none of the asserted references teaches the claimed invention "as a whole" (§ 103(a)) including aspects regarding forming a control gate and a floating gate separated by an interlayer dielectric layer, with spacers that are both arranged and used to mitigate oxygen diffusion to the interlayer dielectric layer. Because none of the references teaches these aspects, no reasonable combination of these references can provide correspondence. As such, the § 103 rejections fail.

As an example, Appellant's specification discusses the formation of multiple spacers around a control gate and interlayer dielectric layer, as well as the use of the spacers to mitigate oxygen diffusion to the interlayer dielectric layer. Accordingly, as shown in Fig. 10 reproduced below, embodiments include multiple spacers 81 surrounding interlayer dielectric 53 and control gate 54.

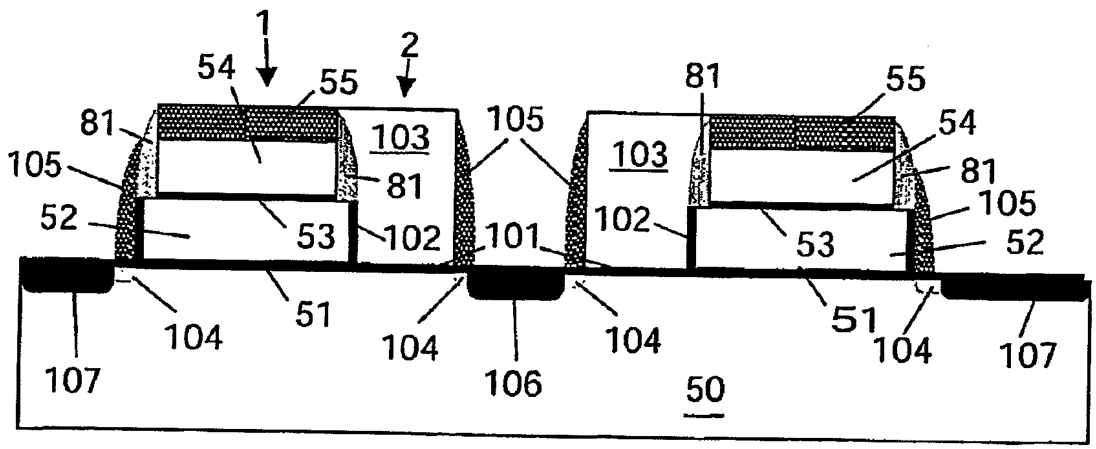

FIG.10

The asserted embodiment of the primary '204 reference, as shown in Fig. 1a reproduced below, includes a single asserted layer 106. Layer 106 is taught to be used to prevent current leakage between a control gate 101 and an erase gate 107. It is undisputed that layer 106 and its use does not correspond to using spacers to mitigate oxygen diffusion to the asserted interlayer dielectric layer 102.

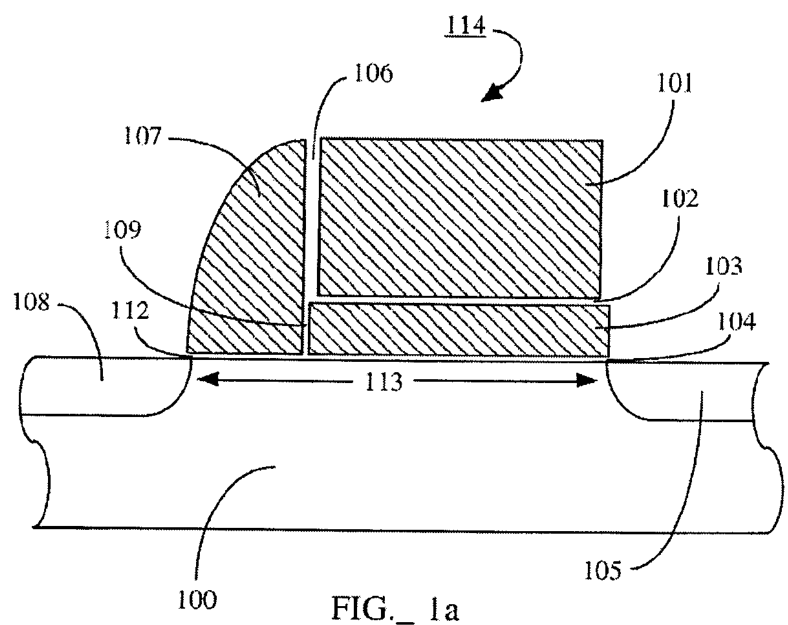

FIG._ 1a

The asserted spacer 106 does not correspond to the plurality of spacers required by the claim language. Further, the Examiner's asserted modification, made clear for the first time in the Advisory Action, of using the spacer material from the '579 reference for spacer 106 does not correct for the lack or correspondence regarding the number of spacers required by the claim language. In addition, the spacer 106 is not used to mitigate oxygen diffusion, nor is the single spacer arranged to mitigate such oxygen diffusion. The asserted embodiment of the '204 reference leaves the interlayer dielectric 102 exposed to the air on the side of the control gate 101 that is not adjacent to the asserted access gate 107.

The Examiner appears to confuse the requirements for assertions of correspondence to an apparatus claim to those of a method claim as the Examiner's assertions of correspondence to the step of using the spacers to mitigate oxygen diffusion appear to be based on an assertion of correspondence to a spacer made of a particular material. The Examiner must show that each step of the method is performed, not that a device with similar characteristics to the end result of the method has been found. The asserted spacers of the '579 reference are not disclosed to mitigate oxygen diffusion, and are not arranged in such a way in the '579 reference that spacers could mitigate oxygen diffusion to an interlayer dielectric. The spacers of the '579 reference are part of an inverted gate structure, where gate oxides 35 and 38 of the '579 reference are completely exposed during any subsequent oxide growth, relative to the asserted spacers 37. The cited spacers 37 therefore do not mitigate the diffusion of oxygen in an interlayer dielectric layer because such layers are formed over the spacer (*e.g.*, tunnel oxide 38 is formed over and after the spacer 37, which thus cannot mitigate any diffusion as asserted). Essentially, the Examiner's rejection relies upon an assertion that *if* the spacers of the '579 reference were arranged in an as yet undisclosed manner to mitigate oxygen diffusion, *then* the cited spacers *could* mitigate oxygen diffusion to an interlayer dielectric material. However, nothing in the record establishes that the purported combination of an inverted-gate structure with the gate stack in the '204 reference would correspond, and nothing in the record suggests arranging the spacers in order to mitigate diffusion (in the context of the method-based limitations or otherwise).

Moreover, the claims at issue are method claims. Any assertions by the Examiner that such limitations are not positive limitations to which correspondence must be shown are

improper. The step of "using" a particular portion of a device being made by the claimed method during the device's manufacture should be afforded the same weight as all other claim limitations. Any position to the contrary is not supported by the M.P.E.P. or relevant case law. *See, e.g.* M.P.E.P. § 2173.05(g).

Various dependent claims include additional references for their rejections. However, nothing in the '746 reference or the '104 reference overcome the deficiencies in the combination of the '204 reference and the '579 reference.

Accordingly, the Examiner's various attempts at asserting correspondence fail as none of the cited references teaches or suggests limitations directed to using spacers to both mask an underlying gate and mitigate the diffusion of oxygen to the deposited interlayer dielectric layer.

2. <u>The Rejection Is Improper For Failing To Provide A Proper Reason To Combine The Asserted References</u>

The Office Action has failed to provide a proper reason to combine the references as asserted. The Examiner's asserted motivation of smoothing topography is not related to the material of the asserted spacer that is relied upon in the rejection, as discussed in more detail below. In addition, incorporation of the portions of the '579 reference responsible for the asserted motivation would result in an hypothetical embodiment inoperable for its intended purpose, contrary to the requirements of the M.P.E.P. and relevant case law.

In presenting a case of obviousness, the Examiner must consider "both the invention and the prior art references as a whole." M.P.E.P. § 2141.02. In addition, "it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does. This is so because inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418-419 (U.S. 2007). The rejections presented by the Examiner appear to combine the material of the spacers of the secondary '579 reference with the gate stack of the flash EEPROM device of the primary '204 reference without regards to overall teachings of either the primary '204

reference or the secondary '579 reference. The present rejection amounts to the assertion that simply finding a spacer made of a material that has an oxygen diffusion, on an order of magnitude smaller than the oxygen diffusion through the oxide spacer, results in the combination being obvious. Allowing such a rejection to stand strips the rejection of any necessary motivation to combine and results in a rejection based on finding the various limitations scattered throughout various references regardless of the actual teachings of the cited references. This is contrary to the M.P.E.P. and relevant case law, including *KSR*.

The Examiner's asserted motivation to combine makes little sense in the context of the primary '204 reference. The Examiner has asserted one would be motivated to combine the references "because the nitride spacer smoothes the topography created by the polysilicon gate and eliminates any sharp corners or edges of polysilicon gate from protruding into overlying layers." The asserted advantage of smoothing the topography is related to the shape of the spacers 37 of the '579 reference, not the nitride material of the spacers. A careful look at the '579 reference indicates that the topography smoothing does not emanate from the material used as the spacer, but rather the shape of spacer used. *See, e.g.*, Figs. 2 and 3. The inclusion of a spacer made of nitride with sharp edges, as shown in Fig. 1a of the '204 reference, on the side of the gate 107 will not smooth the topography of the gate. Further, there is no indication that such a smoothing would be necessary since, unlike the inverted transistor of the '579 reference, there are not layers of material covering the control gate 101 and spacer 106 in the asserted embodiment in Fig. 1a. In addition, should a spacer with the shape disclosed in the '579 reference be used, the spacer would not be able to perform the function of preventing leakage current as required by the '204 reference because portions of the spacer would not be of the thickness needed according to the primary '204 reference.

Accordingly, the Examiner has failed to present a proper case of obviousness under § 103, and Appellant respectfully requests the rejection be overturned.

B. The Rejection Of Claim 6 Is Improper

1. The Examiner Fails To Provide Proper Motivation To Combine The '104 Reference With The '204 Reference, The '579 Reference And The Quirk Reference

The Examiner has failed to provide a proper reason for the inclusion of the teachings of the '104 reference in the asserted hypothetical embodiment. Accordingly to the M.P.E.P. and relevant case law, "rejections on obviousness cannot be sustained with mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *In re Kahn*, 441 F.3d 977, 988, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006) (quoted in *KSR*). The Examiner's asserted reason for including the '104 reference's teachings regarding removing part of the interlayer dielectric layer after forming the control gate is erroneous for two reasons. First, the alleged advantage of the '104 reference is already present in the primary '204 reference. Second, the alleged advantage is unrelated to the aspects of the '104 reference that are relied upon in an attempt to assert correspondence.

The Examiner asserts that one would be motivated to combine the teachings of the '104 reference because the use of the control gate as a mask allows for only one lithographical mask to be used in forming the gate stack. However, the '204 reference already teaches using the control gate as a mask. (*See, e.g.*, the '204 reference, Col. 9:15-16, "etching . . . using control gate poly and floating gate poly as hard masks"). The use of the control gate to limit the number of masks necessary is already a part of the '204 reference. The BPAI has previously held that one having common sense would not look to a secondary reference to solve problem already solved in the primary reference. *See, e.g.*, *Ex Parte Rinkevich et al,* Appeal 20071317, decided May 29, 2007. Accordingly, one of skill in the art would not modify the teachings of the '204 reference with teachings of the '104 reference based on the asserted motivation to combine.

Second, the asserted motivation of the '104 reference relied upon by the Examiner is unrelated to removing interlayer dielectric layer after the control gate is formed, but before the spacers are formed. As shown by the use of the control gate as a mask in the '204 reference, which the Examiner acknowledges does not teach removing part of the interlayer

dielectric layer after forming the control gate but before formation of the spacers, the use of the control gate as a mask does not mean it is used as a mask at a specific time. Accordingly, the Examiner has presented no reason why one would be motivated to remove the interlayer dielectric material as claimed, other than the Appellant's specification and claims.

Accordingly, the asserted reason for combining the '104 reference with the '204 reference lacks proper support, and is illogical. Appellant therefore requests the § 103 rejection of claim 6 be withdrawn.

VIII. Conclusion

In view of the above, Appellant submits that the rejections of claims 1, 3-7, 14 and 17-19 are improper and therefore requests reversal of the rejections as applied to the appealed claims and allowance of the entire application.

Authority to charge the undersigned's deposit account was provided on the first page of this brief.

Please direct all correspondence to:

Corporate Patent Counsel
NXP Intellectual Property & Standards
1109 McKay Drive; Mail Stop SJ41
San Jose, CA 95131

CUSTOMER NO. 65913

By: ______________________
Robert J. Crawford
Reg. No.: 32,122
651-686-6633
(NXPS.442PA)

APPENDIX OF CLAIMS INVOLVED IN THE APPEAL
(S/N 10/574030)

1. A method of manufacturing on a substrate a 2-transistor memory cell comprising a storage transistor having a memory gate stack and a selecting transistor, there being a tunnel dielectric layer between the substrate and the memory gate stack, the method comprising:

forming the memory gate stack by

providing a first conductive layer on the tunnel dielectric layer and a second conductive layer with a deposited interlayer dielectric layer between the first and second conductive layers, the deposited interlayer dielectric layer including oxide and being susceptible to undesirable growth upon exposure to oxygen during subsequent oxidation steps,

etching the second conductive layer thus forming a control gate,

forming spacers against the control gate in the direction of a channel to be formed under the tunnel dielectric layer, the spacers being formed from a dielectric material having an oxygen diffusion through the dielectric material that is, relative to oxide spacers, an order of magnitude smaller than oxygen diffusion through the oxide spacers, and

thereafter using the spacers as a hard mask to etch the first conductive layer thus forming the floating gate, the etching of the first conductive layer being an anisotropic dry etch that is selective to the tunnel dielectric, thereby using the tunnel dielectric to protect portions of the substrate laterally adjacent to the floating gate;

removing a portion of the tunnel dielectric laterally adjacent to the floating gate and exposing a portion of the substrate where the tunnel dielectric has been removed; and

forming an access gate dielectric oxide on the exposed portion of the substrate, using the spacers to mitigate the diffusion of oxygen to the deposited interlayer dielectric layer.

3. A method according to claim 1, wherein the dielectric material having an oxygen diffusion through the material that is an order of magnitude smaller than oxygen diffusion through oxide spacers includes one or more of silicon nitride, silicon carbide or metal oxide.

4. A method according to claim 1, furthermore comprising,

before forming the memory gate stack, applying the tunnel dielectric layer on the substrate, and

after formation of the memory gate stack, removing the tunnel dielectric layer by a selective etching technique at least at a location where the selecting transistor is to be formed, the selective etching technique preferentially etching the tunnel dielectric layer compared to the substrate.

5. A method according to claim 1, further including forming

a floating gate dielectric next to the formed floating gate while forming the access gate dielectric.

6. A method according to claim 1, furthermore comprising

removing part of the interlayer dielectric layer after forming the control gate but before forming the spacers.

7. A method according to claim 1 wherein

forming an access gate includes forming the access gate while the spacer at the access gate side is still present.

14. A method according to claim 1,

wherein removing a portion of the tunnel dielectric includes wet etching the tunnel dielectric to remove a portion of the tunnel dielectric laterally adjacent to the floating gate and expose a portion of the substrate surface where the tunnel dielectric has been wet etched, leaving the exposed surface of the substrate intact, and

further including forming an access gate of the selecting transistor on the access gate dielectric.

17. A method of manufacturing a two-transistor memory cell comprising a storage transistor having a memory gate stack and a selecting transistor, the method comprising:

forming a tunnel dielectric on a substrate;

forming a first conductive layer on the tunnel dielectric;

depositing an interlayer dielectric layer on the first conductive layer, the deposited interlayer dielectric layer including oxide and being susceptible to undesirable growth upon exposure to oxygen during subsequent oxidation steps;

forming a second conductive layer on the interlayer dielectric layer;

etching the second conductive layer to form a control gate;

forming a selecting transistor on the substrate laterally adjacent to the first conductive layer and having an access gate on an access gate dielectric;

forming spacers against sides of the control gate, the spacers being formed from a dielectric material having an oxygen diffusion through the dielectric material that is, relative to oxide spacers, an order of magnitude smaller than oxygen diffusion through the oxide spacers, one of the spacers being formed between the control gate and the access gate;

using the spacers to mask underlying portions of the interlayer dielectric layer and the first conductive layer, etching the first conductive layer to form a floating gate using an anisotropic dry etch that is selective to the tunnel dielectric, using the tunnel dielectric to mask portions of the substrate laterally adjacent to the floating gate;

forming a floating gate sidewall dielectric that is contiguous with the access gate dielectric and present between the floating gate and the access gate, wherein the one of the spacers being formed between the control gate and the access gate is thicker than the floating gate sidewall dielectric;

removing a portion of the tunnel dielectric laterally adjacent to the floating gate and exposing a portion of the substrate where the tunnel dielectric has been removed; and

forming an access gate dielectric oxide on the exposed portion of the substrate, using the spacers to mitigate the diffusion of oxygen to the deposited interlayer dielectric layer.

18. The method of claim 17, further comprising forming a cap layer on the second conductive layer,

wherein forming spacers includes forming the one spacer, which is formed between the control gate and the access gate, between the cap layer and the access gate and in contact with the cap layer, the control gate, the access gate and the floating gate.

19. The method of claim 17, further comprising forming a cap layer on the second conductive layer,

wherein forming spacers includes forming the one spacer, which is formed between the control gate and the access gate, between the cap layer and the access gate and in contact with the cap layer, the control gate, the access gate and the floating gate,

further including forming another floating gate sidewall dielectric located on a sidewall of the floating gate opposite from the floating gate sidewall dielectric, and

further including forming offset spacers, one of the offset spacers being in contact with the access gate, and another one of the offset spacers being in contact with the other floating gate sidewall dielectric and in contact with another one of the spacers that is located on a side of the control gate opposite from the one spacer.

APPENDIX OF EVIDENCE

Appellant is unaware of any evidence submitted in this application pursuant to 37 C.F.R. §§ 1.130, 1.131, and 1.132.

APPENDIX OF RELATED PROCEEDINGS

As stated in Section II above, Appellant is unaware of any related appeals, interferences or judicial proceedings.